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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-----------------|-------------|----------------------|---------------------|------------------|
|-----------------|-------------|----------------------|---------------------|------------------|

10/821,312

04/08/2004

Yu Sun

AMD-H0630

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7590

10/05/2004

WAGNER, MURABITO & HAO LLP

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San Jose, CA 95113

EXAMINER

BOOTH, RICHARD A

ART UNIT

PAPER NUMBER

2812

DATE MAILED: 10/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| | | | |
|------------------------------|-------------------------------|----------------------------|--|
| Office Action Summary | Application No. 10/821,312 | Applicant(s) SUN ET AL. | |
| | Examiner Richard A. Booth | Art Unit 2812 | |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
 - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
 - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
 - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-23 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date. ____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date ____ | 6) <input type="checkbox"/> Other: ____ |

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 2-4, 10-12, and 20-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In each of the above claims, the claims are rendered indefinite because applicant states that the silicon oxide is silicon nitride. Such a statement is confusing because silicon nitride is not a type of silicon oxide but rather they are different materials.

Clarification is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 16 and 20-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Luning et al., U.S. Patent 6,506,642.

Luning et al. shows the invention as claimed including a method for simultaneously manufacturing a semiconductor comprising a wide sidewall spacer and

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a narrow sidewall spacer comprising: depositing a first oxide layer 44 over a first transistor comprising a gate stack 42, a drain side sidewall and a source side sidewall and over a second transistor comprising a gate stack 41, a source side sidewall and a drain side sidewall; etching said first oxide layer wherein a portion of said first oxide layer remains on said source side sidewall and on said drain side sidewall of said first transistor and on said source side sidewall and on said drain side sidewall of said second transistor (see fig. 4); etching said first oxide layer from said source side sidewall of said second transistor 41 (see fig. 5); depositing a second oxide layer over said first transistor and said second transistor; and etching said second oxide layer wherein a portion of said second oxide layer 60 remains on said first oxide layer formed on said source side sidewall and on said drain side sidewall of said first transistor and wherein said second oxide layer remains on said source side sidewall and on said drain side sidewall of said second transistor (see figs. 4-6 and col. 4-line 36 to col. 5-line 19).

Regarding claim 22, note that the etch which removes the first oxide layer from the second transistor is a self-aligned source etch.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Luning et al., U.S. Patent 6,506,642.

Luning et al. is applied as above but fails to expressly disclose wherein said first oxide layer is thicker than said second oxide layer. However, Luning discloses the first oxide layer to be in the range of from 600-1200 angstroms and the second oxide layer to be in the range of from 300-900 angstroms. Therefore, a prima facie case of obviousness exists with respect to the first oxide being thicker than the second oxide because the first oxide layer encompasses a range with larger values than the range of the second oxide layer and overlapping ranges create a prima facie case of obviousness.

Claims 1-5 and 7-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kasai, U.S. Patent 6,352,891 in view of Luning et al., U.S. Patent 6,506,642.

Kasai discloses forming a peripheral transistor with a wide spacer 12 and a core transistor with a narrow spacer 6 (see fig. 6 and its description) but fails to expressly disclose the formation of the spacer structures as claimed.

Luning et al. is applied as above and states that the invention can be applied to a variety of transistors with differing characteristics.

In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Kasai et al. so as to use the process of Luning et al. because this is shown to be an effective method of forming wide and narrow spacers.

Claims 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kasai, U.S. Patent 6,352,891 in view of Luning et al., U.S. Patent 6,506,642 as applied to claims 1-5 and 7-15 above, and further in view of Sun et al., U.S. Patent 5,933,730.

Kasai and Luning et al. are applied as above but fail to expressly disclose wherein the etching to remove the first oxide layer is a self-aligned source etch.

Sun et al. discloses a method in which a self-aligned source etch leads to removal of a spacer in a core area (see fig. 8 and reference numeral 608). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Kasai modified by Luning et al. so as to have the removal of the spacer layer from the core transistor being part of a self-aligned source etch because such a process allows for protection of the core transistor

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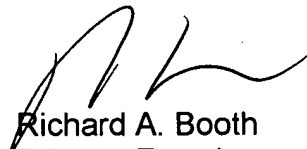
and allows an adequate opening to be formed to allow electrical contact to the source region.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard A. Booth whose telephone number is (571) 272-1668. The examiner can normally be reached on Monday-Thursday from 7:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (571) 272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Richard A. Booth
Primary Examiner
Art Unit 2812

September 29, 2004